AMENDMENTS TO THE SPECIFICATION

Page 1, please replace the paragraph beginning at line 22 with the following rewritten paragraph:

The applicant's patent application (DE 198 02 065.A1), which is a prior application, corresponding to US patent 6,393,078, discloses a method for modulating a basic clock signal for digital circuits and a corresponding clock modulator in which the distances between adjacent switching edges are altered, the respective distance being achieved by virtue of the fact that the basic clock signal is conducted via a changing number of delay units and the distances between the adjacent switching edges are altered in this way.

Page 5, replace the 13 consecutive paragraphs beginning at line 36, with the following 13 consecutive amended paragraphs:

~~x = l * p + a x*t~~

x = I * p + a x*t

where [[l]] I is the interval in which the next switching edge lies, p is the number of possible switching points per half-period T_0 and a is the position of the switching edge in the corresponding interval.

The calculation of the switching edge of the modulated clock signal CM 1 with the modulation factor 1 produces the following for the random number [[1]] I at the beginning of the last switching edge SF 0 with the position a = 0 in the interval 0:

$$a_{i+1} = (0 + 6 - (\frac{5 - 1}{2} - 1) \times 1) \bmod 6 = 5 \bmod 6$$

$$5 = 1 * 6 + 5 * 1$$

$$a_{i+1} = (0 + 6 - (\frac{5 - I}{2} - 1) \times 1) \bmod 6 = 5 \bmod 6$$

$$5 = I * 6 + 5 * 1$$

from this it follows that:

1 = 0 a = 5

I = 0 a = 5

This states that the switching edge SF 1 lies in the same interval at a = 5. If I = 1, the next switching edge lies in the next interval; at I = 2, the switching edge lies in the next interval but one.

The following results for the switching edge SF 2:

$$a_{i+1} = (5 + 6 - (\frac{5 - 1}{2} - 4) * 1) \bmod 6 = 13 \bmod 6$$

$$13 = 1 * 6 + a * 1$$

1 = 2 a = 1

$$a_{i+1} = (5 + 6 - \frac{(5 - I - 4) * 1}{2}) \bmod 6 = 13 \bmod 6$$

$$13 = I * 6 + a * 1$$

$$I = 2 \qquad a = 1$$

This means that the switching edge SF 2 lies in the next interval but one given the value a = 1.

The following results for the switching edge SF 3:

~~$$a_{i+1} = (1 + 6 - \frac{(5 - 1 - 2) * 1}{2}) \bmod 6 = 7 \bmod 6$$~~

~~$$7 = 1 * 6 + a * 1$$~~

~~$$1 = 1 \quad a = 1$$~~

$$a_{i+1} = (1 + 6 - \frac{(5 - I - 2) * 1}{2}) \bmod 6 = 7 \bmod 6$$

$$7 = I * 6 + a * 1$$

$$I = 1 \quad a = 1$$

The following results correspondingly for the switching edge SF 4:

~~$$a_{i+1} = (1 + 6 - \frac{(5 - 1 - 0) * 1}{2}) \bmod 6 = 5 \bmod 6$$~~

~~$$5 = 1 * 6 + a * 1$$~~

~~$$1 = 0 \quad a = 5$$~~

$$a_{i+1} = (1 + 6 - \frac{(5 - I - 0) * 1}{2}) \bmod 6 = 5 \bmod 6$$

$$5 = I * 6 + a * 1$$

$$I = 0 \quad a = 5$$

This means that the switching edge SF 4 lies in the same interval at the location 5.

For the clock signal CM 2 with the modulation factor 2, the following result for the switching edges SF 6 to SF 9:

For the switching edge SF 6:

$$a_{i+1} = \left(0 + 6 - \left(\frac{5 - 1}{2} - 1\right) * 2\right) \bmod 6 = 4 \bmod 6$$

$$4 = 1 * 6 + a * 1$$

$$1 = 0 \qquad a = 4$$

$$a_{i+1} = \left(0 + 6 - \left(\frac{5 - I}{2} - 1\right) * 2\right) \bmod 6 = 4 \bmod 6$$

$$4 = I * 6 + a * 1$$

$$I = 0 \quad a = 4$$

For the switching edge SF 7:

$$a_{i+1} = \left(4 + 6 - \left(\frac{5 - 1}{2} - 4\right) * 2\right) \bmod 6 = 14 \bmod 6$$

$$14 = 1 * 6 + a * 1$$

$$1 = 2 \qquad a = 2$$

$$a_{i+1} = (4 + 6 - \frac{(5 - I - 4) * 2}{2}) \bmod 6 = 14 \bmod 6$$

$$14 = I * 6 + a * 1$$

$$I = 2 \quad a = 2$$

For the switching edge SF 8:

~~$$a_{i+1} = (2 + 6 - \frac{(5 - 1 - 2) * 2}{2}) \bmod 6 = 8 \bmod 6$$~~

~~$$6 = 1 * 6 + a * 1$$~~

~~$$1 = 1 \quad a = 2$$~~

$$a_{i+1} = (2 + 6 - \frac{(5 - I - 2) * 2}{2}) \bmod 6 = 8 \bmod 6$$

$$6 = I * 6 + a * 1$$

$$I = 1 \quad a = 2$$

For the switching edge SF 9:

~~$$a_{i+1} = (2 + 6 - \frac{(5 - 1 - 0) \times 2}{2}) \bmod 6 = 4 \bmod 6$$~~

~~$$4 = 1 * 6 + a * 1$$~~

~~$$1 = 0 \quad a = 4$$~~

$$a_{i+1} = (2 + 6 - \frac{(5 - I - 0) \times 2}{2}) \bmod 6 = 4 \bmod 6$$

$$4 = I * 6 + a * 1$$

$$I = 0 \quad a = 4$$

The block diagram of an exemplary embodiment of the clock modulator according to the invention in Figure 2 has n

series-connected delay units D_1 to D_n with upstream and downstream taps A_0 to A_n connected to a multiplexer 1. The individual delay units D_1 to D_n each generate a delay having the length $t = \frac{2T_0}{n}$ with the result that the complete delay series delays the unmodulated basic clock signal CL present at the input [[6]] E by a total of one period. A calibrating device 2 compares the basic clock signal CL present at the input E with the signal present at the output A_n of the last delay element D_n. If the instants of the switching edges of the two signals do not correspond, the calibrating device 2 calibrates the delay units D_1 to D_n in such a way that the two signals correspond.

Page 10, please replace the paragraph beginning at line 12 with the following rewritten paragraph:

The next random number Z_{i+1} is present at the input 25a, the modulation factor K is present at the input 25b, the constant c is present at the input 26a and the position a_i of the preceding switching edge SF, which is read from the register 28, is present at the input 26b. The product from the multiplier 25 and the sum from the adder 26 are summed in the adder 27 to give a sum S. The highest bit of this sum S is passed to the set input of the lock flip-flop 30, the second highest bit is passed to the input of the toggle flip-flop 29, and the two remaining, lower bits are passed to the register 28. The output of the register 28 drives the two multiplexers ~~25, 26~~ 20, 21 and is furthermore fed back to an input of the adder 26.

Page 11, please replace the paragraph beginning at line 19 with the following rewritten paragraph:

The modulation begins with the value 3 in the register 28, the random number $Z_i = 1$ and the outputs of the flip-flops 29, 30 shall be at 0. If the value 0 is present at the input of the multiplexer 22, the latter switches through to the multiplexer 20, and to the multiplexer 21 in the case of the value 1. The 3 means that the input TAPP3 and respectively TAPN3 of the multiplexer[[s]] 21 is switched through, with the result that the signal which is present downstream of the delay unit D3 is switched through, which signal, upon its next positive edge, will switch over the output of the toggle flip-flop 23.